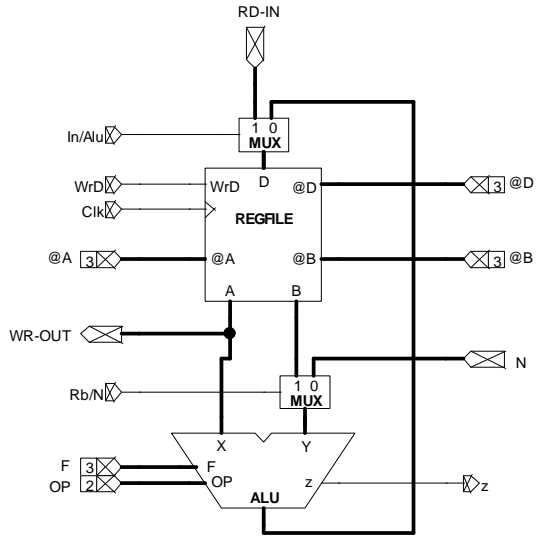


### UPG básica



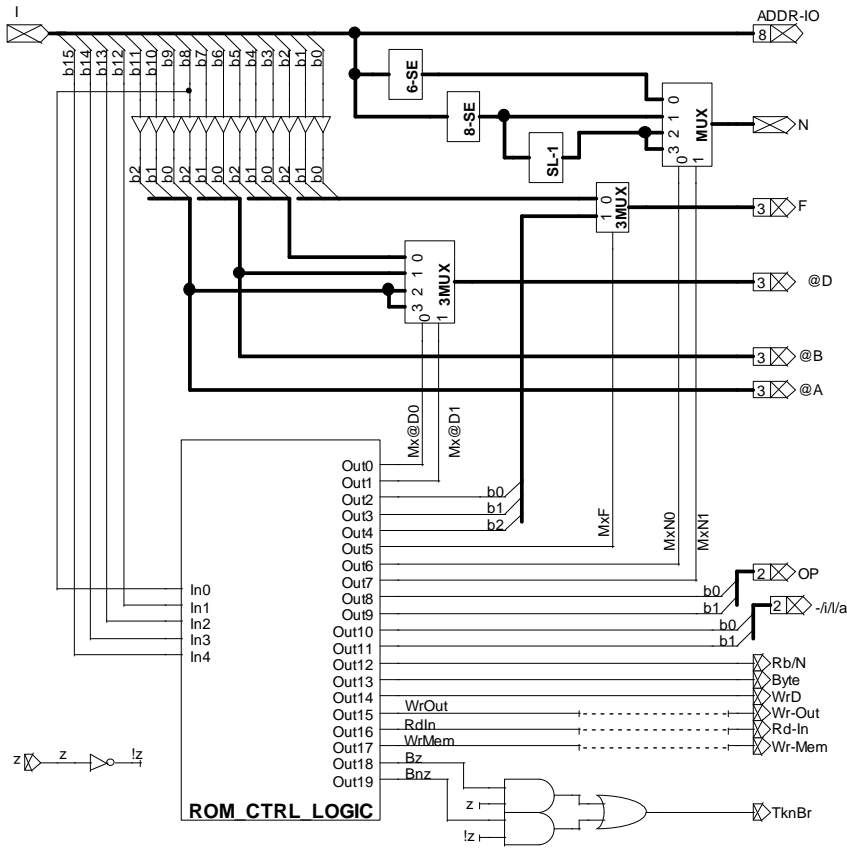
### Formato Instrucciones SISA-I

15 14 13 12	11 10 9	8 7 6	5 4 3	2 1 0	Name	Mnemonic
0 0 0 0	a a a	b b b	d d d	f f f	Logic and Arithmetic Operations	AND, OR, XOR, NOT, ADD, SUB, SHA, SHL
0 0 0 1	a a a	b b b	d d d	f f f	Compare Signed and Unsigned	CMPLT, CMPLE, -, CMPEQ, CMPLTU, CMPLEU, -, -
0 0 1 0	a a a	d d d	n n n n n n n		Add Immediate	ADDI
0 0 1 1	a a a	d d d	n n n n n n n		Load	LD
0 1 0 0	a a a	b b b	n n n n n n n		Store	ST
0 1 0 1	a a a	d d d	n n n n n n n		Load Byte	LDB
0 1 1 0	a a a	b b b	n n n n n n n		Store Byte	STB
0 1 1 1					Branch future extension	
1 0 0 0	a a a	0 1	n n n n n n n		Branch on Zero	BZ
	d d d	0 1	n n n n n n n		Branch on Not Zero	BNZ
1 0 0 1	a a a	0 1	n n n n n n n		Move Immediate	MOVI
	d d d	1	n n n n n n n		Move Immediate High	MOVHI
1 0 1 0	d d d	0 1	n n n n n n n		Input	IN
	a a a	1	n n n n n n n		Output	OUT
1 0 1 1					Future extensions	
1 1 x x					Future extensions	

### Funcionalidades ALU

F	OP			
	b <sub>2</sub> b <sub>1</sub> b <sub>0</sub>	11	10	01
0 0 0	---	X	CMPLT (X,Y)	AND(X,Y)
0 0 1	---	Y	CMPLE (X,Y)	OR(X,Y)
0 1 0	---	MOVHI (X,Y)	---	XOR(X,Y)
0 1 1	---	---	CMPEQ (X,Y)	NOT(X)
1 0 0	---	---	CMPLTU (X,Y)	ADD(X,Y)
1 0 1	---	---	CMPLEU (X,Y)	SUB(X,Y)
1 1 0	---	---	---	SHA(X,Y)
1 1 1	---	---	---	SHL(X,Y)

### Lógica de control del SISC Harvard Uniciclo



### Computador SISC Harvard Uniciclo (UCG + UPG + IO + MEM)

